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(54) **Integrated circuit including a resistive element**

(57) An integrated circuit includes a resistive element in which a high-sheet-resistivity zone (11) connects two spaced-apart zones (12, 13). A conductive field plate (15) overlies the high-sheet-resistivity zone (11) and is insulated from it by a composite insulating layer (16, 17). The field plate (15) is connected to a node of the circuit and stabilises the resistance of the element by inhibiting depletion or inversion of surface regions of the high-sheet-resistivity zone (11). A suitable node is one (13) of the spaced-apart zones, preferably the one which in use is the more negative, in the case of a P-type high-sheet-resistivity zone. The invention is particularly applicable to linear integrated circuits where stable resistances are required.

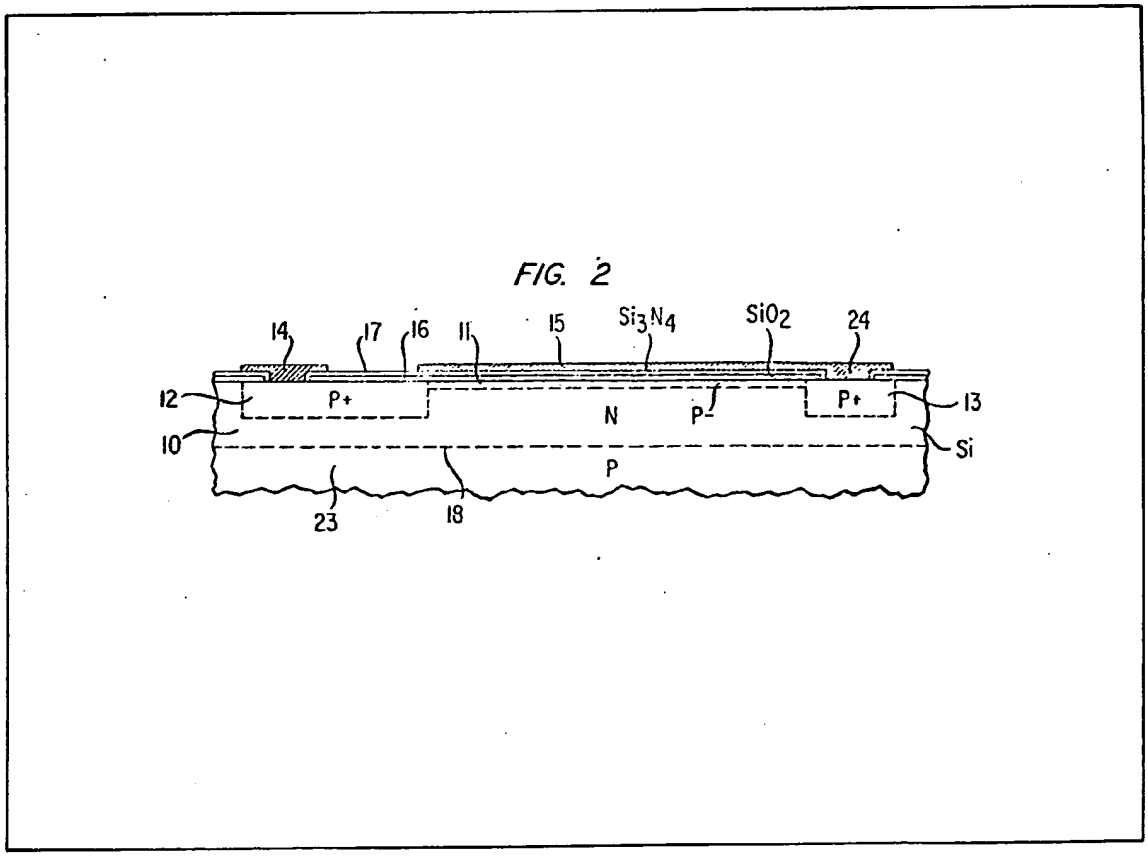

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FIG. 1

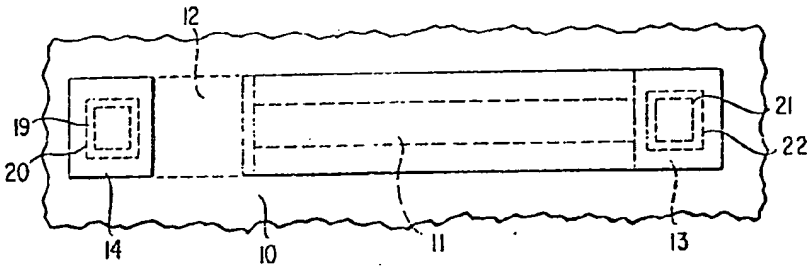


FIG. 2

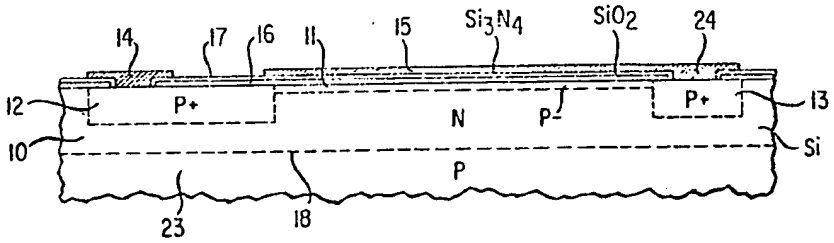
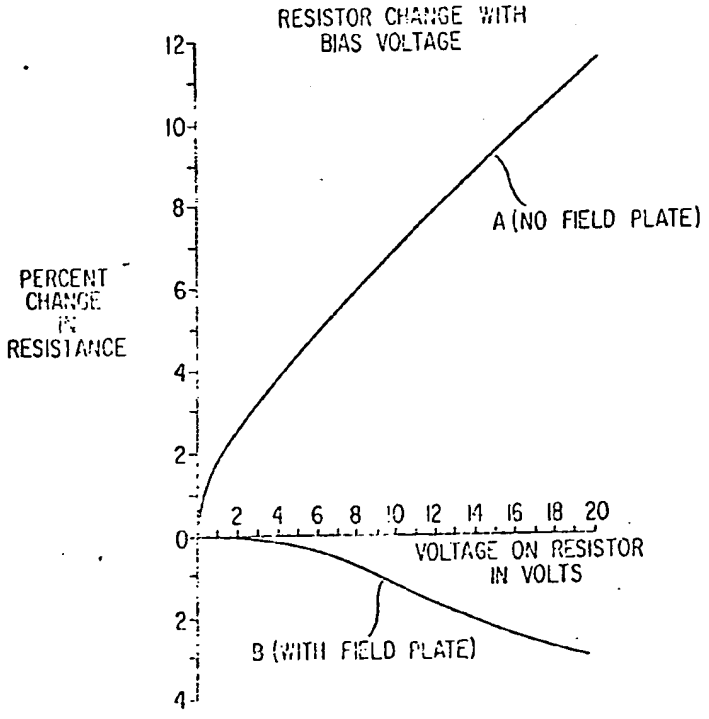


FIG. 3



SPECIFICATION

Integrated circuit including a resistive element

This invention relates to semiconductor integrated circuits including resistance elements.

Resistors are customarily formed in semiconductor integrated circuits by defining therein a conductivity type zone of relatively high resistivity to which a pair of low resistance connections are made. One problem with such integrated circuit resistors, particularly those of high value, formed typically by ion implantation, is an undesired change in resistance value which is a function both of time and the voltage across the PN junction between the conductivity type zone defining the resistor and the adjoining portion of the semiconductor body. In a specific example, a resistor fabricated by ion implantation in a silicon semiconductor body with a sheet resistance of about 2000 ohms per square exhibited a change in resistance value of more than ten percent with a voltage change from zero to twenty volts. In many integrated circuit devices, resistors may show continuing change or drift in resistance value with the application of bias voltage over a period of time. Although in some circuits compensation may be provided, the nonlinearity of the drift and the time factor render such efforts generally inadequate. In semiconductor integrated circuits of the linear type where precise high value resistors are important, resistance drift significantly degrades the circuit performance.

In the invention as claimed the resistance of a resistive element is stabilised by means of a conductive field plate which overlies entirely the boundaries of the conductivity type zone constituting the resistive element. Although the cause of drift in resistance value is not completely understood, it appears to stem from a redistribution of charge on the surface of the silicon resistor. An ionic species on the surface of the silicon nitride dielectric passivation layer depletes or even inverts the surface of the lightly-doped resistor thereby increasing its value. Accordingly, the provision of a field plate suitably connected to a node of the circuit appears to inhibit such depletion or inversion. More particularly, by connecting the field plate electrically to the terminal of the resistor which in use is downstream with respect to majority carrier flow in the resistor (i.e. the more negative terminal in the case of P-type conductivity), the voltage coefficient of the resistor is opposed and compensated for.

No significant change in the fabrication processes for the integrated circuit is necessary to provide the field plate. For example a simple mask change may be made to enable formation of the metal field plate overlying the usual insulating films on the semiconductor surface simultaneously with the formation of the metal inter-connection pattern.

An embodiment of the invention will now be described by way of example with reference to the accompanying drawing in which:—

FIG. 1 is a plan view of a portion of a semiconductor integrated circuit showing the layout of a resistor in accordance with the invention;

FIG. 2 is a side elevation in section of the portion of the integrated circuit including the resistor of FIG 1; and

FIG. 3 is a graph illustrating the change in resistance of a silicon resistor with applied voltage with and without the compensating field plate.

In FIGS. 1 and 2 the same reference numerals are used for identical features insofar as possible and this description will make reference to both figures.

In this specific embodiment the semiconductor body comprises single crystal silicon, and, in accordance with the current practice, comprises an N-type conductivity layer 10 formed epitaxially by vapour deposition growth on a starting portion 23 of P-type conductivity. The use of an epitaxial layer, however, is not essential to this invention. The high value ion-implanted resistor of interest in connection with this invention comprises the high resistivity layer 11 of P-type conductivity. The layer 11 terminates in a pair of high conductivity type (P+) zones 12 and 13. The length of the zone 11 between bones 12 and 13 constitutes the length of the resistor.

It should be noted that the resistor need not necessarily have the rectilinear shape illustrated but may be formed in another pattern, such as the meandering configurations well known in the art for increasing the length of a resistor within a given area.

Overlying the silicon surface is a layer of silicon dioxide 16 which is further covered by a layer of silicon nitride 17 to provide the customary protective and passivating coatings. Openings 19 and 21 are provided to both P+ conductivity type terminal zones 12 and 13 through which are formed the metallic conductive contacts 14 and 24 making electrical connection to the resistor. Metallic contact 14 contacts zone 12 and may be further connected by conductive metal patterns, not shown, to other portions of the circuit. Boundaries 20 and 22 indicate the somewhat larger openings made in the underlying silicon dioxide layer. Metallic contact 24 is connected to terminal zone 13 at the other end of the resistor and to the conductive layer 15 which entirely overlies the boundaries of the P conductivity type zone 11. Accordingly, the field plate 15 is connected to one end of the resistor 11. Thus the voltage applied at terminal end zone 13 is the voltage applied to the field plate 15, which thereby acts to suppress the tendency of the silicon surface thereunder to deplete or even invert with respect to surface charge. Moreover, in this particular embodiment terminal zone 13 may be taken as the more negative end of the resistor so that the field plate induced voltage counters the voltage coefficient existing as a consequence of the voltage drop from one end of the resistor to the other with bias.

Referring to FIG. 3, the advantageous effect of the field plate is illustrated by the contrast between the measured effects shown by curves A and B. In particular, in the absence of the compensating field plate, curve A, a change in resistance of almost 12 percent was observed as the bias voltage on the resistor was increased from 0 to 20 volts. These observations were made using suitably cleaned specimens, and the voltage was read immediately

after application of bias. At 10 volts it should be noted that the percent change is almost 7 percent. With the compensating field plate, curve B, on the other hand, the percent change in resistance value up to 20 volts bias was about 3 percent, and at 10 volts was about 1 percent. Moreover, the use of the field plate dramatically suppresses the drift in resistance with the passage of time. This change in resistance obviously has a seriously degrading effect on integrated circuits, particularly of the linear type in which the stability of resistors of the type of interest herein is critical with respect to the operation of the circuit.

In a typical embodiment, following the formation of the epitaxial layer 10, the integrated circuit is fabricated in conventional fashion including the formation of the P+ conductivity type zones 12 and 13 which may coincide with the step in which, for example, the base zones of the transistors of the circuit are formed. The P– conductivity type zone 11 constituting the resistor is formed advantageously by ion implantation which enables the precise relatively shallow doping of this zone. In particular, resistors of interest in connection with this invention have sheet resistivities of from about 500 to about 2000 ohms per square. Such resistors may have impurity concentrations of from about 2×10^{13} atoms per square centimetre to about 1×10^{14} atoms per square centimetre. Specifically, for an epitaxial layer of from 2 to 4 ohm centimetres resistivity, a boron ion implantation dosage of 2.6×10^{13} atoms per square centimetre at 30 kV will provide a sheet resistivity of about 2000 ohms per square. The terminal zones 12 and 13 of P+-type conductivity typically have a peak doping concentration of about 5×10^{19} and are much deeper than the shallow resistor zone 11. Typically, resistor zone 11 may have a depth of about 0.2 microns. Although the particular dopants used are not critical, the P+ zones conventionally are formed using boron and the N-type zones may be phosphorus, antimony or arsenic doped.

Because of the shallow resistor zone, the silicon dioxide film 16 is relatively thin, about 200 Ångström units. It may be formed, typically, by heating the body in dry oxygen at about 900 degrees Centigrade for about twenty minutes. The silicon nitride layer 17 typically is about 2000 Angstrom units thick and is formed by the usual pyrolytic deposition process.

The overlying conductive film, referred to heretofore as metal, may be conductive polycrystalline silicon or a single metal such as aluminium or aluminium with underlying titanium or, as in this specific embodiment, a system in which sintered platinum forms an intimate contact of platinum silicide to the silicon surface where such contact is required, the surface then being overlaid in turn by layers of titanium, platinum or palladium, and gold.

The insulating film may be of silicon dioxide or, as in this specific embodiment, a layer of silicon dioxide covered by a layer of silicon nitride.

CLAIMS

1. A semiconductor integrated circuit comprising a semiconductor body and including a resistive element comprising a first surface zone of a first conductivity type, having a sheet resistivity of at least 500 ohms per square and connecting a pair of spaced apart zones of comparatively low resistivity and of the first conductivity type, the first zone being isolated from the remainder of the body except for the spaced apart zones by a PN junction bounding the first zone, and a conductive layer insulatedly overlying the whole of the first zone, the conductive layer being electrically connected to a node of the integrated circuit so as to form a field plate operative to stabilise the resistance value of the resistive element.

2. An integrated circuit as claimed in claim 1, wherein the node to which the conductive layer is connected is one of the spaced apart regions.

3. An integrated circuit as claimed in claim 1, wherein the node to which the conductive layer is connected is that one of the spaced apart regions which when the integrated circuit is in use is downstream with respect to majority carrier flow in the first zone.

4. An integrated circuit as claimed in claim 3, wherein the first conductivity type is P-type and the one of the spaced apart regions to which the conductive layer is connected is that one which in use is the most negative electrically.

5. An integrated circuit as claimed in any of the preceding claims, wherein the semiconductor is silicon and the conductive layer is insulated from the first zone by a composite layer comprising a layer of silicon dioxide formed on a surface of the body including the first zone and a layer of silicon nitride formed on the layer of silicon dioxide.

6. An integrated circuit as claimed in claim 5, where the silicon dioxide layer has a thickness of about 200 Ångström units and the silicon nitride layer has a thickness of about 200 Ångström units.

7. An integrated circuit including a resistive element substantially as herein described with reference to FIGS. 1 and 2 of the accompanying drawings.

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